UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,358	02/06/2002	Kenneth C. Duisenberg	10019681-1	4285

7590 01/29/2007

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/072,358	DUISENBERG, KENNETH C.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection. Objection of claim 6 due to informality is withdrawn. Currently claims 1-24 are pending for examination.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-17 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Lounsbury et al. (US Patent 4,637,023).

5. As per claims 1, 10 and 16, AAPA teaches a data processing flow control computer system and method comprising:

a processor (Specification, p. 1, ll. 10-11);

a ring of buffers (Drawings, Fig. 1 and Specification, p. 1, l. 17);

a computer readable memory coupled to said processor implementing a method of processing data (Specification, p. 1, ll. 16-34), comprising:

receiving an interrupt indicating data from a local area network (LAN) has been stored in one of a plurality of buffers and is ready for processing (Specification, p. 1, ll. 19-21);

if a software buffer index points to a first buffer containing processed data as the LAN software check and finds the processed data, the LAN software waits and the software buffer index is not advanced to the next buffer (Specification, p. 3, ll. 9-15);

if the software buffer index points to the first buffer containing unprocessed data (Specification, p. 1, ll. 21-22), as the LAN software check and finds the new data to process, the unprocessed data is processed by the LAN software and the software buffer index is advanced to the next buffer (Specification, p. 4, ll. 24-26);

sequentially processing the plurality of subsequent buffers if the LAN software continue to check and find unprocessed data in the subsequent buffers, then advancing

the software buffer index after processing the unprocessed data, wherein the checking, finding and processing of unprocessed data is implemented until the LAN software check and finds processed data in the subsequent buffer (Specification, p. 4, ll. 24-30); and

when the software buffer index is synchronized to a hardware buffer index, after processing the unprocessed data, the software buffer index is reset to a next available buffer having processed data (Specification, p. 3, l. 33 to p. 4, l. 9).

AAPA does not teach the data processing flow control computer system and method comprising:

searching through the plurality of buffers containing data to determine whether there is a second buffer with unprocessed data, if the software buffer index points to the first buffer containing processed data; and

if there is said second buffer with unprocessed data, synchronizing said software buffer index to a hardware buffer index by resetting said software buffer index to a next available buffer having processed data following said second buffer, and otherwise stopping said searching when each buffer of said plurality of buffers has been searched and a buffer with unprocessed data is not found.

Lounsbury teaches a system and a method comprising:

transferring data between a peripheral and a host computer via a ring of buffers (col. 13, ll. 3-47): and

when an error occurs while transferring the data from the ring of buffers to the host computer, the ring of buffers is sequentially searched for the correct data to

continue transferring, and stop the searching if the correct data is not found after searching all the buffers in the ring of buffers (col. 13, l. 18-41 and col. 18, l. 41-52).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Lounsbury's searching of the ring of buffers into AAPA's data processing flow control. The resulting combination of the references further teaches the data processing flow control computer system and method comprising:

when the error occurs as the software buffer index pointing to the first buffer containing processed, the ring of buffers is sequentially searched for a second buffer with the unprocessed data (e.g. correct data);

if the second buffer with the unprocessed data was found, the software buffer index would synchronize with the hardware buffer index, as the detected unprocessed data and any subsequent unprocessed data would be processed until the software buffer index reaches the buffer with processed data, therefore resetting the software buffer index to the next available buffer having processed data following the second buffer; and

stopping the searching of the second buffer with the unprocessed data (e.g. correct data) if the unprocessed data is not found after searching all the buffers in the ring of buffers.

Therefore, it would have been obvious to combine Lounsbury with AAPA for the benefit of providing a robust method for transferring data between the peripheral and the host computer via the ring of buffers, by correcting the error as data is transferred

from the ring of buffers to the host computer are corrected (Lounsbury, Abstract; col. 13, ll. 18-41 and col. 18, ll. 41-52).

6. As per claims 2 and 17, AAPA and Lounsbury teach all the claimed limitations of claims 1 and 16 as discussed above, where AAPA further teaches the data processing flow control computer system and method wherein said synchronizing further comprises synchronizing hardware buffer index and said software buffer index in response to an interrupt indicating data has been stored in one of said plurality of buffers and is ready for processing (AAPA, Specification, p. 1, ll. 19-21).

7. As per claims 4, 13 and 19, AAPA and Lounsbury teach all the claimed limitations of claims 1, 10 and 16 as discussed above, where AAPA further teaches the data processing flow control computer system and method comprises determining if said first buffer contains processed data; and processing data in said first buffer if said data is unprocessed (AAPA, Specification, p. 1, ll. 21-22), as the LAN software check the buffer index and find the new data to process.

8. As per claims 5 and 20, AAPA and Lounsbury teach all the claimed limitations of claims 1 and 16 as discussed above, where AAPA further teaches the data processing flow control computer system and method wherein said synchronizing further comprises wrapping around to a start buffer (AAPA, Drawings, Buffer 0 of Fig. 1) after searching the end buffer in said plurality of buffers when sequentially searching through said

plurality of buffers, said plurality of buffers sequentially beginning with the start buffer (AAPA, Drawings, Buffer 0 of Fig. 1) and ending with an end buffer (AAPA, Drawings, Buffer N of Fig. 1) (AAPA, Specification, p. 1, ll. 23-26 and p. 4, ll. 20-33).

9. As per claims 6, 14 and 21, AAPA and Lounsbury teach all the claimed limitations of claims 1, 10 and 16 as discussed above, where both further teach the data processing flow control computer system and method further comprises:

when said software buffer index points to said first buffer containing processed data, using a value of said software buffer index corresponding to said first buffer as a reference value (Lounsbury, col. 18, ll. 41-52), wherein it would have been obvious to utilize the value of the software buffer index as the reference point in order to properly determine if all the buffers in the ring of buffers have been searched;

incrementing said software buffer index as each buffer of said plurality of buffers is searched, wherein when said software buffer index reaches one end of a range of possible values it is reset to the other end of said range (AAPA, Drawings, Fig. 1; Specification, p. 1, ll. 23-26 and p. 4, ll. 27-33); and

stopping said searching when said software buffer index reaches said reference value without finding a buffer in said plurality of buffers with unprocessed data (Lounsbury, col. 18, ll. 41-52).

10. As per claims 7 and 22, AAPA and Lounsbury teach all the claimed limitations of claims 1 and 16 as discussed above, where AAPA further teaches the data processing

flow control computer system and method further comprises wherein each of said plurality of buffers is a local area network (LAN) buffer for storing LAN packets of data (AAPA, Specification, p. 1, ll. 33-34).

11. As per claims 8 and 23, AAPA and Lounsbury teach all the claimed limitations of claims 7 and 22 as discussed above, where AAPA further teaches the data processing flow control computer system and method further comprises wherein said software buffer index is a LAN software buffer index, and said hardware buffer index is a LAN hardware buffer index (AAPA, Specification, p. 1, ll. 28-29).

12. As per claim 9, 15 and 24, AAPA and Lounsbury teach all the claimed limitations of claims 1, 10 and 16 as discussed above, where AAPA further teaches the data processing flow control computer system and method further comprises processing said unprocessed data in said second buffer (AAPA, Specification, p. 1, ll. 21-22 and p. 4, ll. 20-33), as the LAN software check the buffer index and find the new data to process.

13. As per claim 11, AAPA and Lounsbury teach all the claimed limitations of claim 10 as discussed above, where AAPA further teaches the data processing flow control computer system and method further comprises wherein said data from said LAN is a LAN packet (AAPA, Specification, p. 1, ll. 33-34).

14. As per claim 12, AAPA and Lounsbury teach all the claimed limitations of claim 10 as discussed above, where AAPA further teaches the data processing flow control computer system and method further comprises wherein a LAN driver performs said receiving, said searching and said synchronizing (AAPA, Specification, p. 1, ll. 12-14).

15. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Lounsbury et al. (US Patent 4,637,023), and further in view of Cromer et al. (US Patent 5,860,001).

AAPA and Lounsbury teach all the claimed limitations of claims 1 and 16 as discussed above, where AAPA further teaches the data processing flow control computer system and method comprising synchronizing the hardware buffer index and the software buffer index in response to a first interrupt indicating data has been stored in one of said plurality of buffers and is ready for processing when the software buffer index points to the first buffer containing processed data (AAPA, Specification, p. 1, ll. 19-21).

AAPA and Lounsbury do not teach the data processing flow control computer system and method wherein said synchronizing further comprises ignoring the first interrupt indicating data has been stored in one of said plurality of buffers and synchronizing said hardware buffer index and said software buffer index in response to a second interrupt indicating data has been stored in one of said plurality of buffers.

Cromer teaches the computer system and method comprising wherein there are at least two boot sequences and wherein the boot sequence after the computer is

turned on comprising of loading BIOS, the operating system and the particular application defined by initialization control information which causes an initial program load (IPL) (col. 1, l. 28 to col. 2, l. 64), therefore upon turning on the computer system, said computer system requires a period of time before reaching a state of stability wherein the properly initialization has been completed (Fig. 10-11).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Cromer's plurality of boot sequences into AAPA and Lounsbury's data processing flow control. The resulting combination of the references further teaches the data processing flow control computer system and method wherein said synchronizing further comprises ignoring the first interrupt because the computer system requires the period of time before reaching the state of stability; and synchronizing the hardware buffer index and the software buffer index in response to a second interrupt indicating data has been stored in one of said plurality of buffers and is ready for processing when the software buffer index points to said first buffer containing processed data for a second time, as the state of stability is reached.

Therefore, it would have been obvious to combine Cromer with AAPA and Lounsbury for the benefit of providing the easier method for managing the computer system (Cromer, col. 1, l. 28 to col. 2, l. 64 and col. 11, ll. 14-23).

IV. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-24 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 22, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER